**IN THE CLAIMS**:

Please amend the claims as follows:

1. (Withdrawn) A clock switching circuit that switches between asynchronous first and second clocks according to whether an interface cable, having a hot-plug function, is connected or disconnected and comprising:

a first flip-flop group that receives an interface disconnection signal that corresponds to a disconnection or connection of the interface cable in response to said first clock, wherein when the interface cable is disconnected, a final-stage flip-flop thereof outputs a first selection signal through a number of first clock edges which correspond to a first stage number of the first flip-flop group, and when said interface cable is connected, the final-stage flip-flop outputs a first no-selection signal through one time of the first clock edge, said first flip-flop group outputting said first clock in response to said first selection signal, and prohibiting output of said first clock in response to said first no-selection signal;

a second flip-flop group that receives said interface disconnection signal in response to said second clock, wherein when said interface cable is connected, the final-stage flip-flop thereof outputs a second selection signal through a number of second clock edges which correspond to a second stage number of the second flip-flop group, and when said interference cable is disconnected, the final-stage flip-flop outputs a second no-selection signal through one time of the second clock edge, said second flip-flop group outputting said second clock in response to said second selection signal,

and prohibiting output of said second clock in response to said second no-selection signal; and

where the second stage number of said second flip-flop group is greater than the first stage number of said first flip-flop group according to a relationship between the frequency of said first and second clocks.

2. (Withdrawn) The clock switching circuit of claim 1 wherein;

said second clock is supplied from a PLL circuit that generates said second clock from said first clock, and

when said interface cable is connected, operation of said PLL circuit starts in response to said interface disconnection signal, and said interface disconnection signal is received by said second flip-flop group after a set time therefrom.

3. (Withdrawn) The clock switching circuit of claim 2 wherein;

when said interface cable is disconnected, operation of said PLL circuit stops in response to said interface disconnection signal.

4. (Withdrawn) The clock switching circuit of claim 1 wherein;

the second stage number of said second flip-flop group is changed according to the operating clock frequency of said interface cable to be connected.

5. (Currently Amended) A method for controlling a clock switching circuit, comprising:

receiving a basic clock signal from an outside;

receiving a PLL clock signal generated by a PLL circuit based on the basic clock signal, said PLL clock signal being faster than the basic clock;

receiving a switch signal for switching an output from the basic clock signal to the PLL clock signal;

inhibiting outputting the basic clock signal upon receiving a connection of an interface cable which transmits a high speed signal ~~the switch signal~~;

counting a predetermined number of the PLL clock signal after inhibiting outputting the basic clock signal; and

outputting the PLL clock signal after the number of the PLL clock signal, wherein the predetermined number is set according to the frequency difference between the basic clock frequency and the PLL clock frequency.

6. (Withdrawn) A clock switching circuit that switches between a basic clock signal and a PLL clock signal generated by a PLL circuit, said PLL clock signal being faster than the basic clock signal, comprising:

a first flip-flop group having a first number of flip-flop circuits, that receives the basic clock signal and outputs an outputted basic clock signal;

a second flip-flop group having a second number of flip-flop circuits, that receives the PLL clock signal and outputs an outputted PLL clock signal; and

a selecting circuit that selects either one of the outputted basic clock signal or the outputted PLL clock signal;

wherein the second number is greater than the first number according to a relationship between the frequency of said basic clock signal and said PLL clock signal so as to prevent the clock switching circuit from producing a hazard.

7. (Currently Amended) A clock signal switching circuit that switches an output from a basic clock to a fast clock comprising:

a PLL circuit that generates said fast clock whose frequency is more than twice as much as a frequency of the basic signal; and

an inhibiting circuit that selects said fast clock in response to a connecting of an interface cable which transmits a high speed signal and inhibits said [[first]] fast clock in response to a disconnecting of the interface cable which transmits a high speed signal,

wherein said inhibiting circuit includes:

a first circuit for disappearing the basic clock as the output when the switching said output from said basic clock to said fast clock, and

a second circuit for inhibiting the fast clock until the basic clock disappears through the first circuit and for allowing the output of the fast clock when the switching said output from said basic clock to said fast clock.

8. (Currently Amended) A clock signal switching circuit that switches an output from a basic clock to a fast clock comprising:

a PLL circuit that generates said fast clock whose frequency is more than twice as much as a frequency of the basic signal; and

an inhibiting circuit that inhibits said fast clock in response to a connecting of an interface cable within a term which depends on a difference between said frequency of said basic clock and said frequency of said fast clock in the case of switching said output from said basic clock to said fast clock,

wherein said inhibiting circuit includes:

a first circuit for disappearing the basic clock as the output when the switching said output from said basic clock to said fast clock, and

a second circuit for inhibiting the fast clock until the basic clock disappears through the first circuit and for allowing the output of the fast clock when the switching said output from said basic clock to said fast clock.